WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a memory cell storing data; and

a word line and a pair of bit lines connected to said memory cell; wherein

said memory cell includes

a first inverter including a first load element and a first driving element having an N channel MOS transistor,

a second inverter cross-coupled with said first inverter, including a second load element and a second driving element having another N channel MOS transistor,

first and second storage nodes connected respectively to output nodes of said first and second inverters, and

first and second gate elements each including a P channel MOS transistor having a gate electrode connected to said word line, connecting said first and second storage nodes to one bit line and the other bit line of said pair of bit lines, respectively;

a first metal interconnection forming said first storage node is provided stacked on said first driving element and said first gate element formed on a substrate surface;

a second metal interconnection forming said second storage node is provided stacked on said second driving element and said second gate element formed on said substrate surface; and

said first and second load elements are provided above said first and second metal interconnections

2. The semiconductor memory device according to claim 1, wherein

each of said first and second metal interconnections is formed of metal having heat resistance to processing temperature when said first and second load elements are formed.

3. The semiconductor memory device according to claim 2, wherein

each of said first and second load elements includes a P channel thin film transistor.

4. The semiconductor memory device according to claim 2, wherein each of said first and second load elements includes a resistance element formed of polysilicon and having a resistance value higher than a prescribed resistance value.

5. The semiconductor memory device according to claim 2, wherein each of said first and second metal interconnections is formed of metal having lower resistance than a gate electrode material of said first and second gate elements.

6. The semiconductor memory device according to claim 5, wherein each of said first and second metal interconnections is formed of tungsten.

7. The semiconductor memory device according to claim 1, wherein said first metal interconnection connects drain electrode of said first gate element, drain electrode of said first driving element and gate electrode of said second driving element with each other;

said second metal interconnection connects drain electrode of said second gate element, drain electrode of said second driving element and gate electrode of said first driving element with each other; and

said first and second load elements are formed over said first and second metal interconnections with an interlayer insulating film interposed, and connected respectively to said first and second metal interconnections through first and second connecting portions.

8. The semiconductor memory device according to claim 7, further comprising

a plurality of first barrier layers provided at contact portions between said first or second metal interconnection and respective ones of

said plurality of drain electrodes having heat resistance to processing temperature when said first or second load element is formed.

9. The semiconductor memory device according to claim 8, wherein each of said plurality of first barrier layers is formed of cobalt silicide or nickel silicide.

10. The semiconductor memory device according to claim 8, further comprising

a plurality of connection layers provided between each of said plurality of first barrier layers and the corresponding first or second metal interconnection, forming an ohmic contact between said corresponding first or second metal layer and the corresponding drain electrode.

11. The semiconductor memory device according to claim 10, wherein

each of said plurality of connection layers is formed of titanium silicide.

12. The semiconductor memory device according to claim 10, further comprising

a plurality of second barrier layers provided between each of said plurality of connection layers and said corresponding first or second metal interconnection, protecting the corresponding connection layer and/or the corresponding first barrier layer when said corresponding first or second metal interconnection is formed.

13. The semiconductor memory device according to claim 12, wherein

each of said plurality of second barrier layers is formed of titanium nitride.

14. The semiconductor memory device according to claim 10,

wherein

each of said first barrier layers has diffusion coefficient in said corresponding drain electrode smaller than the diffusion coefficient of the corresponding connection layer in said corresponding drain electrode.

15. The semiconductor memory device according to claim 7, wherein

each of said first and second load elements includes a P channel thin film transistor; and

planes facing said P channel thin film transistor in said first and second metal interconnections are planarized.

16. The semiconductor memory device according to claim 7, wherein

each of said first and second load element includes a resistance element formed of polysilicon and having a resistance value higher than a prescribed resistance value; and

planes facing said resistance element in said first and second metal interconnections are planarized.

17. The semiconductor memory device according to claim 1, further comprising:

an internal power supply generating circuit receiving an external power supply voltage and generating an internal voltage lower than a prescribed voltage; wherein

said memory cell operates with said internal voltage generated by said internal power supply generating circuit.

18. The semiconductor memory device according to claim 17, wherein

said prescribed voltage is 3V.

19. The semiconductor memory device according to claim 1, wherein said memory cell further includes

a first capacitance element having one terminal connected to said

first storage node and the other terminal connected to a node with a constant potential, and

a second capacitance element having one terminal connected to said second storage node and the other terminal connected to said node with the constant potential.